PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) **International Patent Classification:** **G03F 7/20**	**A1**	(11) **International Publication Number:**	**WO 00/67074**
		(43) **International Publication Date:**	09 November 2000 (09.11.2000)

(21) **International Application Number:** PCT/US00/05658

(22) **International Filing Date:** 03 March 2000 (03.03.2000)

(30) **Priority Data:**
09/302,561 30 April 1999 (30.04.1999) US

(60) **Parent Application or Grant**
MENTOR GRAPHICS, INC. [/]; (). COBB, Nicolas, Bailey [/]; (). AUYEUNG, Aloysuis, T., C. ; ().

Published

(54) **Title: STREAMLINED IC MASK LAYOUT OPTICAL AND PROCESS CORRECTION THROUGH CORRECTION REUSE**

(54) **Titre: CORRECTIONS RATIONALISEES DES DISTORSIONS DUES AU TRAITEMENT ET DES DISTORSIONS OPTIQUES PERMETTANT LE TRACE D'UN MASQUE DE CIRCUIT INTEGRE ET INTEGRANT DES CORRECTIONS ANTERIEURES**

(57) Abstract

An EDA tool is provided with an OPC module that performs optical and/or process pre-compensations on an IC mask layout in a streamlined manner, reusing determined corrections for a first area on a second area, when the second area is determined to be equivalent to the first area for OPC purposes. The OPC module performs the correction on the IC mask layout on an area-by-area basis, and the corrections are determined iteratively using model-based simulations, which in one embodiment, include resist model-based simulations as well as optical model-based simulations.

(57) Abrégé

L'invention se rapporte à un outil d'automatisation de conception électronique (EDA) comportant un module de précompensations optiques (OPC) qui effectue, de manière rationalisée, des précompensations optiques et/ou de traitement lors du tracé d'un masque de circuit intégré, en réutilisant, pour une seconde zone, des corrections déterminées précédemment pour une première zone, lorsque ladite seconde zone est évaluée comme étant équivalente à la première zone s'agissant de l'application de précompensations optiques. Le module OPC effectue la correction sur le tracé du masque de circuit intégré, zone après zone, et les corrections sont déterminées de manière itérative, au moyen de simulations fondées sur un modèle, qui incluent, dans une réalisation de l'invention, des simulations fondées sur un modèle de résine ainsi que des simulations fondées sur un modèle optique.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : G03F 7/20

A1

(11) International Publication Number: **WO 00/67074**

(43) International Publication Date: 9 November 2000 (09.11.00)

(21) International Application Number: PCT/US00/05658

(22) International Filing Date: 3 March 2000 (03.03.00)

(30) Priority Data:
09/302,561 30 April 1999 (30.04.99) US

(71) Applicant: MENTOR GRAPHICS, INC. [US/US]; 8005 S.W. Boeckman Road, Wilsonville, OR 97070 (US).

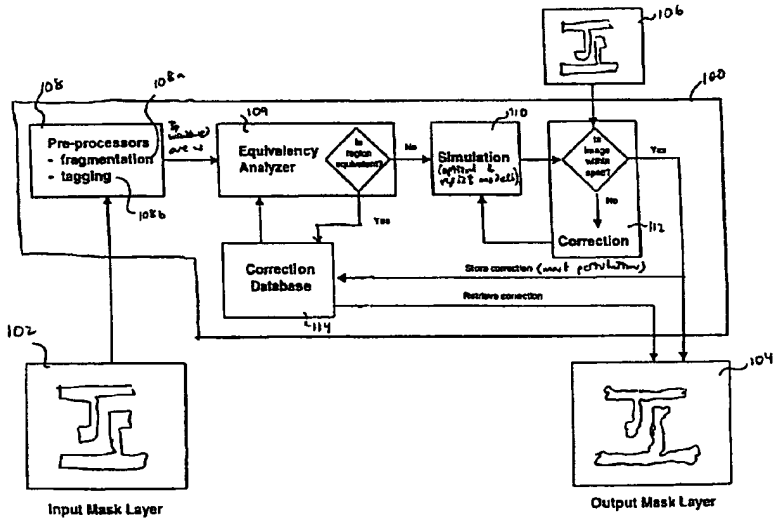
(72) Inventor: COBB, Nicolas, Bailey; 1632 Willow Lake Lane, San Jose, CA 95131 (US).

(74) Agents: AUYEUNG, Aloysuis, T., C. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025–1026 (US).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: STREAMLINED IC MASK LAYOUT OPTICAL AND PROCESS CORRECTION THROUGH CORRECTION REUSE



(57) Abstract

An EDA tool is provided with an OPC module that performs optical and/or process pre–compensations on an IC mask layout in a streamlined manner, reusing determined corrections for a first area on a second area, when the second area is determined to be equivalent to the first area for OPC purposes. The OPC module performs the correction on the IC mask layout on an area–by–area basis, and the corrections are determined iteratively using model–based simulations, which in one embodiment, include resist model–based simulations as well as optical model–based simulations.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

D scription

5

10

15

20

25

30

35

40

45

50

55

Streamlined IC Mask Layout Optical And Pro ess Correction Through Correction Reuse

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of integrated circuit (IC) design. More specifically, the present invention relates to the application of optical and process pre-compensations to an IC mask layout.

2. Background Information

Over the years, because of the ever increasing complexity of IC designs, IC designers have become more and more reliant on electronic design automation (EDA) tools to assist them in designing ICs. These tools span the entire design process, from synthesis, placement, routing, to layout verification.

In the case of sub-micron ICs, designers are increasingly reliant on EDA tools to make the necessary pre-compensations (also referred to as corrections) to the edges of various geometries of an IC mask layout, to achieve the desired sub-micron IC images, as the "critical dimension" of the line-width becomes smaller than the wavelength of the light source. (The term mask as used herein is intended to include reticle also.) The various techniques for automatically making these corrections are commonly referred to as optical proximity corrections or optical and process corrections. In the later case, pre-compensations are made for process as well as optical distortions. Whether it is just for optical distortions only or for both types of distortions, hereinafter, all pre-compensations will be generically referred to as OPC.

Generally speaking, OPC techniques can be classified as rule-based techniques or model-based techniques. Under rule-based techniques, certain

predetermined corrections are made if certain pre-specified conditions are detected, e.g. when certain geometric features are employed in the presence of certain other features within certain critical distances. Under model-based techniques, the corrections are calculated through computer simulations employing various models, e.g. optical models. Thus, generally speaking, rule-based techniques are less accurate, but they are less computational intensive. On the other hand, model-based techniques are more accurate, but they are more computationally intensive. Furthermore, for certain large ICs, some model-based techniques border on impractical, as they require very powerful computing systems. Therefore, designers of complex ICs are often faced with this difficult choice of accuracy versus computational efficiency.

Thus, a more streamlined model-based OPC technique that offers the desired improved accuracy but with less of the computational burden is desired.

SUMMARY OF THE INVENTION

An EDA tool is provided with an OPC module that performs optical and/or process pre-compensations on an IC mask layout in a streamlined manner, reusing determined corrections for a first area on a second area, when the second area is determined to be equivalent to the first area for OPC purposes. The OPC module performs the correction on the IC mask layout on an area-by-area basis, and the corrections are determined iteratively using model-based simulations, which in one embodiment, include resist model-based simulations as well as optical model-based simulations.

BRIEF DESCRIPTION OF DRAWINGS

The present invention will be described by way of exemplary embodiments, but not limitations, illustrated in the accompanying drawings in which like references denote similar elements, and in which:

Figure 1 illustrates an overview of the present invention in accordance with one embodiment;

Figure 2 illustrates the concept of fragmenting an edge of a geometry feature of an IC mask layout;

Figures 3a-3b illustrate the concept of windowed area for OPC analysis;

Figure 4 further illustrates a correction database in accordance with one embodiment;

Figure 5 illustrates the operational flow of the OPC module in accordance with one embodiment;

Figure 6 illustrates an example EDA tool incorporated with the OPC module of the present invention, in accordance with one embodiment; and

Figure 7 illustrates an example computer system suitable to be programmed with the programming instructions implementing the EDA tool of **Fig. 6**.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, various aspects of the present invention will be described, and various details will be set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some or all aspects of the present invention, and the present invention may be practiced without the specific details. In other instances, well known features are omitted or simplified in order not to obscure the present invention.

Parts of the description will be presented using terminology commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art, such as mask layouts, geometries, model-based simulations and so both. Also, parts of the description will also be presented in terms of operations performed by a computer system, using terms such as determining, generating and so forth. As well understood by those skilled in the art, these operations and quantities operated on, take the form of electrical, magnetic, or optical signals

capable of being stored, transferred, combined, and otherwise manipulated through electrical/optical components of a digital system; and the term digital system includes general purpose as well as special purpose data processing machines, systems, and the like, that are standalone, adjunct or embedded.

Various operations will be described as multiple discrete steps performed in turn in a manner that is most helpful in understanding the present invention. However, the order of description should not be construed as to imply that these operations are necessarily performed in the order they are presented, or even order dependent. Lastly, repeated usage of the phrase "in one embodiment" does not necessarily refer to the same embodiment, although it may.

Referring now to **Figure 1**, wherein a block diagram illustrating an overview of the present invention in accordance with a number of embodiments is shown. Shown is OPC module **100** incorporated with the teachings of the present invention, which includes automatic performance of OPC to IC mask layout **102**, on an area-by-area basis, to generate corrected IC mask layout **104**. In particular, OPC module **100** reuses corrections determined for a first area on a second area, when the second area is considered to be equivalent to the first area for OPC purposes. As a result, the amount of computations required to perform OPC on IC mask layout **102** to generate IC mask layout **104** are substantially reduced.

For the illustrated embodiment, OPC module **100** includes a number of pre-processors **108**, equivalency analyzer **109**, simulator **110**, correction post-processor **112**, and correction database **114**, operationally coupled to each other as shown. Pre-processors **108** include in particular, fragmentation pre-processor **108a** and tagging pre-processor **108b**. Pre-processors **108** collectively pre-process the formal description of IC mask layout **102** to prepare the descriptive data for the subsequent analyses to determine the appropriate correction. In particular, pre-processors **108** collectively prepare the descriptive data to enable the subsequent analyses to be efficiently performed in accordance with the

streamlined approach of the present invention, that is allowing the determined corrections for one area to b efficiently reused for another OPC equivalent area. Equivalency analyzer **109** performs pattern recognition analysis to determine if two areas are "equivalent" for OPC purposes, on an area-by-area basis. If equivalent, analyzer **109** further causes the earlier determined corrections to be reused on the area to avoid repeating the costly re-computations. Simulator **110** performs for each "unique" area, model-based analyses to determine the appropriate corrections for the particular "unique" area. Correction post-processor **112** makes the determined corrections for each area. For each "unique" area, the simulation and correction process is performed multiple times, iteratively, referencing desired results **106**, until the corrected mask layout is considered to be sufficiently pre-compensated that it is likely to yield the desired image, within a predetermined tolerance level. Correction database **114** stores the data necessary to allow two areas to be compared and determined whether they are equivalent for OPC purposes. Furthermore, correction database **114** stores the data necessary to allow the corrections determined for one area to be reused for another area, when the latter area is determined to be equivalent to the former area for OPC purposes.

Continuing to refer to **Fig. 1**, for the illustrated embodiment, IC mask layout **102** is described in GDS II format, comprises of polygons and paths, more specifically, vertices of polygons and paths, among other things. Fragmentation pre-processor **108a** takes each edge of the geometries, and injects additional "vertices" to further fragment the edge into multiple edge segments or fragments, for analysis purpose, thereby improving the resolution of the subsequent analyses performed to determine the appropriate corrections (see. **Fig. 2**). As those skilled in the art will appreciate, such injection of additional vertices and fragmentation of the edges into multiple edge fragments result in substantial increase in computational cost for the subsequent simulation analyses. As will be described in more details below, to alleviate this substantial increase in computational cost for the improved accuracy, equivalency analyzer **109** advantageously ensures the costly computations are performed only once for each OPC "unique" area, and

reuses the determined corrections on equivalent areas, from an OPC perspective. To facilitate efficient performance of the equivalent analysis by analyzer **109**, tagging pre-processor **108b** employs tag identifiers to characterize the geometric features of each area of IC mask layout **102**. Examples of tag identifiers are identifiers that characterize an edge fragment as a vertical edge fragment, a horizontal edge fragment, an edge fragment adjacent to a line end edge fragment, a concave corner edge fragment, and so forth. Tagging is the subject of co-pending application, number <to be inserted>, entitled "Improved Method and Apparatus For Sub-micron IC Design Using Edge Fragment Tagging", and filed contemporaneously with the present application, which is hereby fully incorporated by reference.

For the illustrated embodiment, equivalency analyzer **109** efficiently performs the equivalent analysis on an "windowed area"-by-"windowed area" basis. A windowed area encircles and includes an original area. The windowed area is created by enlarging the perimeter of the original area by an encircling ring of immediately adjacent areas to be included for OPC analysis. The size of the encircling ring is defined by a window dimension (d_w). Geometry features disposed within this encircling area are considered to be significant from an OPC analysis point of view (see **Fig. 3a-3b**). In alternate embodiments, different d_w may be employed for different enlargement directions. Analyzer **109** compares the geometric features of a windowed area against the geometric features of a previously corrected windowed area (in its pre-correction state), using the tag identifiers tagged against the edge fragments by tagging pre-processor **108b**. In one embodiment, two windowed areas are considered equivalent if and only if the two areas are identical in all aspects, that is the number, size and relative locations of the geometric features. In other embodiments, two windowed areas are considered equivalent if the two windowed areas have the same number of geometric features, and the sizes and relative locations of the geometric features are all within predetermined tolerance levels. In yet other embodiments, other criteria may be employed instead to determine equivalency. Simulator **110** performs the simulation analyses for the windowed unique areas of IC mask

layout **102**, using both resist as well as optical models. In one embodiment, the resist mod l employed is a variable threshold resist (VTR) model.

Finally, correction database **114** is employed to store the description data of each windowed OPC unique area of an IC mask layout, and the corrected state of each of these windowed OPC unique areas (see **Fig. 4**). In an alternate embodiment, in lieu of the corrected state of each of these windowed OPC unique areas, the corrections, also referred to as mask perturbations, to be made to each of the windowed OPC unique area are stored instead. In yet another embodiment, both the corrections, i.e. the mask perturbations, as well as the corrected states of the windowed OPC unique areas are stored.

Except for the advantageous employment of correction database **114** to store the data necessary, and their usage to reuse corrections determined through simulations for one area on another area that is considered to be OPC equivalent to the earlier area, pre-processors **108** (exclusion of tagging pre-processor **108b**), simulator **110** and correction post processors **112**, (exclusion of equivalency analyzer **109**) have been otherwise previously described in detail in Cobb et al., "Large area phase-shift mask design", In Proceedings of SPIE Symposium on Optical Microlithography, Vol. 2197, pages 348-360, 1994; Cobb et al., "Fast low complexity mask design", In Proceedings of SPIE Symposium on Optical Microlithography, Vol. 2440, pages 313-327, 1995; Cobb et al., "Fast sparse aerial image calculation for OPC", In Proceedings of BACUS Symposium on Photomask Technology", Vol. 2621, pages 534-545, 1995; Cobb et al., "A Mathematical and CAD framework for Proximity Correction", In Proceedings of SPIE Symposium on Optical Microlithography, Vol. 2726, pages 348-360, 1996; and Cobb et al., "Experimental Results on Optical Proximity Corrections with Variable Threshold Resist Model", In Proceedings of SPIE Symposium on Optical Microlithography X, Vol. 3051, pages 458-468, 1997. These articles are hereby fully incorporated by reference.

Referring now to **Figur 5**, wherein a flow diagram illustrating th operational flow of the above described OPC module in accordance with one embodiment is shown. (The parenthesized reference numbers refer to elements of **Fig. 1**.) As illustrated, at **502**, the fragmentation pre-processor (**108a**) fragments edges and the tagging pre-processor (**108b**) tags edge fragments of an IC mask layout (**102**). At **504**, the equivalency analyzer (**109**) selects a windowed area of the IC mask layout for analysis. The order of analysis is unimportant. In one embodiment, it is systematic, in another, it is arbitrary. At **506**, the analyzer (**109**) determines if the windowed area is equivalent to a previously corrected windowed area. For the illustrated embodiment, the analyzer (**109**) retrieves the descriptive data of the pre-correction state of a previously corrected windowed area from a correction database (**114**). The equivalent analysis is efficiently performed using the tag identifiers applied by tagging pre-processor (**109**).

If the windowed area is determined to be OPC equivalent to a previously corrected area, the process continues at **508**, where the analyzer (**109**) merely causes the previously determined corrections to be reused on the area to avoid the necessity having to re-perform the timely simulations. In one embodiment, the analyzer (**109**) causes the corrected state of the previously corrected area to be retrieved and output from correction database (**114**). In another embodiment, the analyzer (**109**) causes the previous determined corrections or mask perturbations to be retrieved from correction database (**114**) and applied to the IC mask layout (**102**) by correction post-processor (**112**).

On the other hand, if the windowed area is determined to be non-equivalent to any of the previously corrected areas, from an OPC perspective, the process continues at **510**, where the simulator (**110**), in conjunction with correction post-processor (**112**), iteratively determines the corrections to be made. Upon determining and applying the determined corrections, at **514**, simulator (**110**) and correction post-processor (**112**) further save the data necessary for the determined corrections to be subsequently reused on another OPC equivalent windowed area. Simulator (**110**) and/or correction post-processor (**112**) save the

descriptive data of the pre-c rrection state of the windowed area into corr ction database (**114**). Additionally, in one embodiment, correction post-processor (**112**) also saves the corrected state of the windowed area. In another embodiment, correction post-processor (**112**) saves the corrections to be applied instead. In yet another embodiment, correction post-processor (**112**) saves both.

From operation **508** or **514**, the process continues at **516**, where analyzer (**109**) determines if all areas have been processed. Analyzer (**109**) repeats the process from operation **504** through operation **514**, selectively invoking simulator (**110**) and correction post-processor (**112**) as many times as it is necessary, until all areas of IC mask layout (**102**) have been processed and corrected.

Referring now to **Figure 6**, wherein an EDA tool incorporated with the OPC module of the present invention in accordance with one embodiment is shown. As illustrated, EDA tool suite **600** includes OPC module **602** incorporated with the teachings of the present invention as described earlier with references to **Fig. 1-5**. Additionally, EDA tool suite **600** includes other tool modules **604**. Examples of these other tool modules **602** include but not limited to synthesis module, phase assignment module, layout verification module and so forth.

Figure 7 illustrates one embodiment of a computer system suitable for use to practice the present invention. As shown, computer system **700** includes processor **702** and memory **704** coupled to each other via system bus **706**. Coupled to system bus **706** are non-volatile mass storage **708**, such as hard disks, floppy disk, and so forth, input/output devices **710**, such as keyboard, displays, and so forth, and communication interfaces **712**, such as modem, LAN interfaces, and so forth. Each of these elements perform its conventional functions known in the art. In particular, system memory **704** and non-volatile mass storage **708** are employed to store a working copy and a permanent copy of the programming instructions implementing the above described teachings of the present invention. System memory **704** and non-volatile mass storage **706** may

also be employed to store the IC designs. The permanent copy of the programming instructions to practice the present invention may be loaded into non-volatile mass storage **708** in the factory, or in the field, using distribution source/medium **714** and optionally, communication interfaces **712**. Examples of distribution medium **714** include recordable medium such as tapes, CDROM, DVD, and so forth. In one embodiment, the programming instructions are part of a collection of programming instructions implementing EDA tool **600** of **Fig. 6**. The constitution of elements **702-714** are well known, and accordingly will not be further described.

In general, those skilled in the art will recognize that the present invention is not limited to the embodiments described. Instead, the present invention can be practiced with modifications and alterations within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative, instead of restrictive on the present invention.

Thus, a streamlined approach to performing optical and process corrections to an IC mask layout, through correction reuse, has been described.

Claims

CLAIMS

What is claimed is:

1. A method for performing OPC on an IC mask layout comprising:

determining OPC for the IC mask layout on an area-by-area basis, each area being an aerial subset of the IC mask layout;

reusing the determined OPC for a first area on a second area if the second area is considered to be equivalent to the first area for OPC purposes.

2. The method of claim 1, wherein said OPC for each area is determined iteratively employing model-based simulations.

3. The method of claim 2, wherein said model-based simulations include resist as well as optical model-based simulations.

4. The method of claim 3, wherein each of said resist model-based simulations employs a variable threshold resist model.

5. The method of claim 2, wherein each of said model-based simulations includes geometries of an adjacent neighboring area that are within an enlargement distance from the area for which the model-based simulation is being performed.

6. The method of claim 1, wherein the method further comprises determining if each area is equivalent to any one of the previously corrected areas, prior to the application of the corrections, for OPC purposes.

7. The method of claim 6, wherein the method further comprises selectively tagging geometries of each area with tag identifiers to characterize the geometries to facilitate efficient performance of said equivalency determination.

8. The method of claim 1, wherein the method further comprises saving the determined OPC, and pre-correction states of the corresponding corrected areas.

9. The method of claim 8, wherein said reusing comprises retrieving for the second area, the saved OPC determined for the first area, and applying the retrieved OPC to the second area.

10. The method of claim 1, wherein the method further comprises saving the corrected areas in their corrected states as well as their pre-correction states.

11. The method of claim 10, wherein said reusing comprises retrieving for the second area, the corrected first area in its corrected state, and generating a copy for use as the corrected second area.

12. An article of manufacture comprising

a recordable medium having recorded thereon programming instructions for use to program a computer system to enable the computer system to be able to determine OPC for an IC mask layout on an area-by-area basis, each area being an aerial subset of the IC mask layout, and to reuse the determined OPC for a first area on a second area if the second area is considered to be equivalent to the first area for OPC purposes.

13. The article of claim 12, wherein said programming instructions enable the computer system to determine the OPC for each area iteratively employing model-based simulations.

14. The article of claim 13, wherein said programming instructions enable the computer system to include resist as well as optical model-based simulations when performing said model-based simulations.

15. The article of claim 14, wherein said programming instructions enable the computer system to employ a variable threshold resist model when performing a resist model-based simulation.

16. The article of claim 13, wherein said programming instructions enable the computer system to include, when performing a model-based simulation, geometries of an adjacent neighboring area that are within an enlargement distance from the area for which the model-based simulation is being performed.

17. The article of claim 12, wherein said programming instructions further enable the computer system to determine if each area is equivalent to any one of the previously corrected areas, prior to the application of the corrections, for OPC purposes.

18. The article of claim 17, wherein said programming instructions further enable the computer system to selectively tag geometries of each area with tag identifiers to characterize the geometries to facilitate efficient performance of said equivalency determination.

19. The article of claim 12, wherein said programming instructions further enable the computer system to save the determined OPC, and pre-correction states of the corresponding corrected areas.

20. The article of claim 19, wherein said programming instructions enable the computer system to retrieve for the second area, the saved OPC determined for the first area, and to apply the retrieved OPC to the second area.

21. The article of claim 12, wherein said programming instructions further enable the computer system to save the corrected areas in their corrected states as well as their pre-correction states.

22. The article of claim 21, wh rein said programming instructions further enable the computer system to retri ve for the second area, the corrected first area in its corrected state, and to generate a copy for use as the corrected second area.

23. A computer system comprising:

a storage medium having stored therein a plurality of programming instructions; and

a processor coupled to the storage medium to execute the programming instructions to determine OPC for an IC mask layout on an area-by-area basis, each area being an aerial subset of the IC mask layout, wherein the determined OPC for a first area are reused on a second area if the second area is considered to be equivalent to the first area for OPC purposes.

24. The computer system of claim 23, wherein the processor executes the programming instructions to iteratively determine the OPC for each area employing model-based simulations.

25. The computer system of claim 24, wherein the processor executes the programming instructions to perform resist as well as optical model-based simulations.

26. The computer system of claim 25, wherein the processor executes the programming instructions to perform the resist model-based simulations employing a variable threshold resist model.

27. The computer system of claim 24, wherein the processor executes the programming instructions to perform a model-based simulation for an area, including geometries of an adjacent neighboring area that are within an enlargement distance from the area for which the model-based simulation is being performed.

28. The computer system of claim 23, wherein the processor executes the programming instructions to determine if each area is equivalent to any one of the previously corrected areas, prior to the application of the corrections, for OPC purposes.

29. The computer system of claim 28, wherein the processor executes the programming instructions further to selectively tag geometries of each area with tag identifiers to characterize the geometries to facilitate efficient performance of said equivalency determination.

30. The computer system of claim 23, wherein the processor further executes the programming instructions to save the determined OPC, and pre-correction states of the corresponding corrected areas.

31. The computer system of claim 30, wherein the processor further executes the programming instructions to retrieve for the second area, the saved OPC determined for the first area, and to apply the retrieved OPC to the second area.

32. The computer system of claim 23, wherein the processor further executes the programming instructions to save the corrected areas in their corrected states as well as their pre-correction states.

33. The computer system of claim 32, wherein the processor further executes the programming instructions to retrieve for the second area, the corrected first area in its corrected state, and to generate a copy for use as the corrected second area.

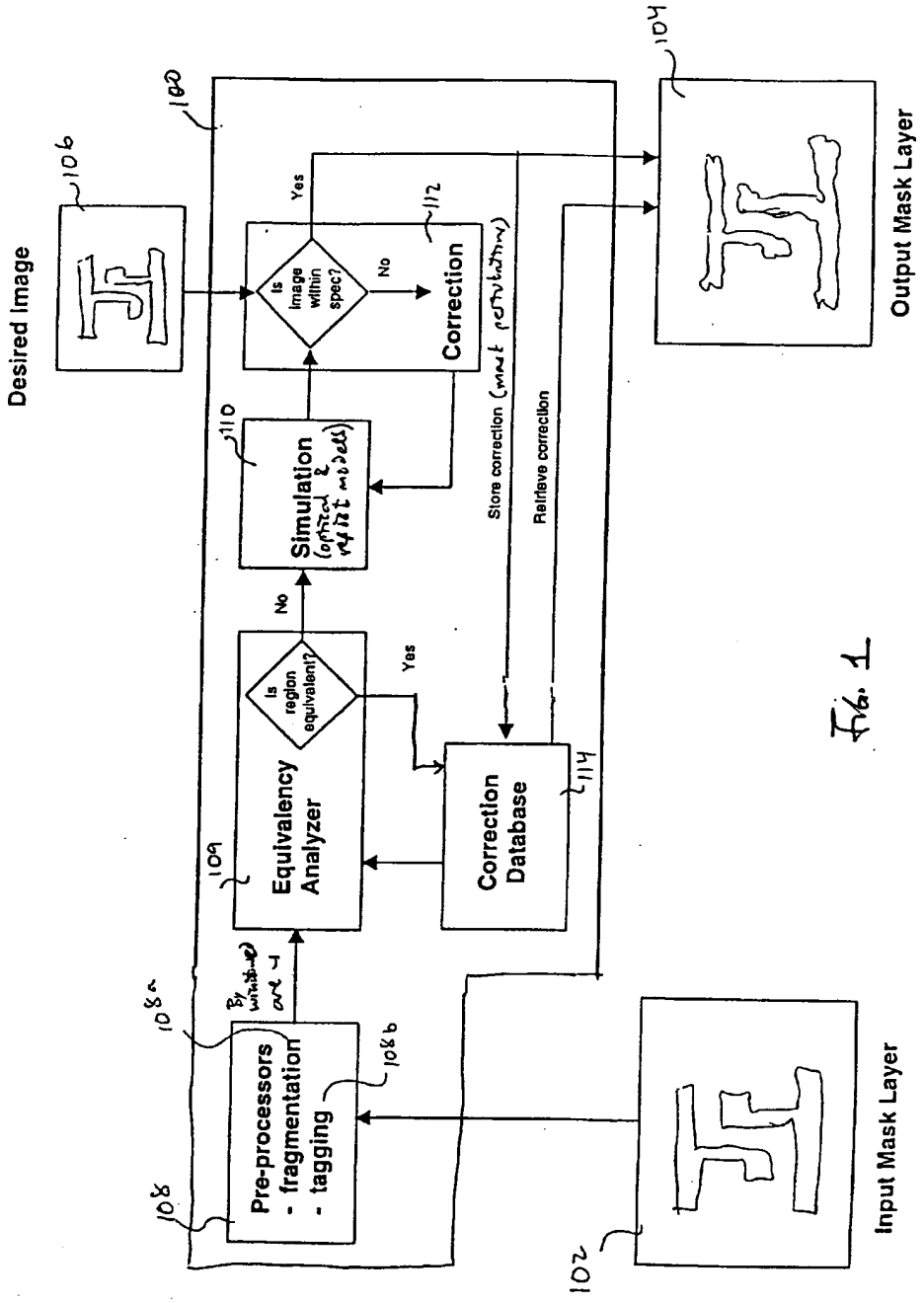

Desired Image
Is Image within spec?
Yes
No
Correction
Simulation
Is region equivalent?
No
Yes
Equivalency Analyzer
Correction Database
Store correction
Retrieve correction
Pre-processors
- fragmentation
- tagging
Output Mask Layer
Input Mask Layer

Fig. 1

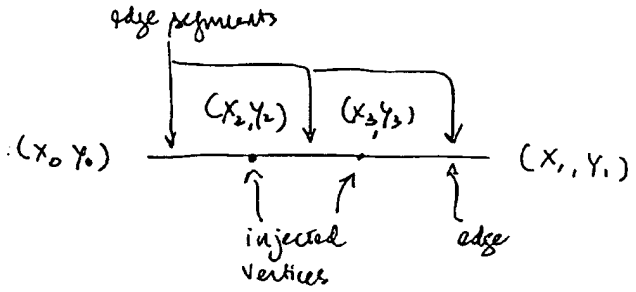


Fig. 2

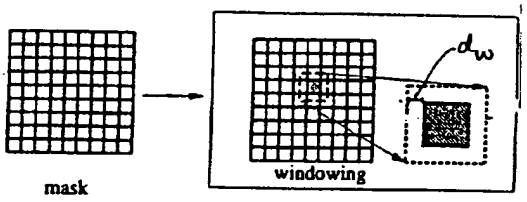


Fig. 3a

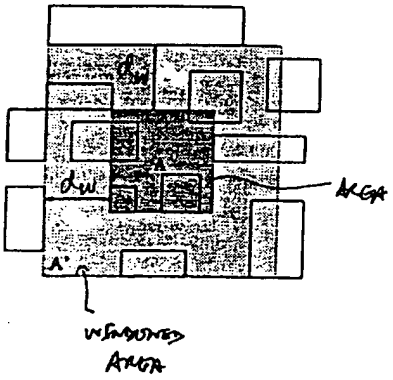


Fig. 3b

CORRECTION DATABASE

UNCORRECTED WINDOWED AREA	CORRECTED WINDOWED ±
{ POLY1(X1,Y1, X2,Y2 ··· TAG1), PATH1 (X3,Y3 ··· TAG2), POLY2 (X4,Y4 ··· TAG3) .... }	{ POLY'1 (X'1,Y'1, Y PATH1 (X'3,Y'3 POLY'2 (X ...

Fig. 4

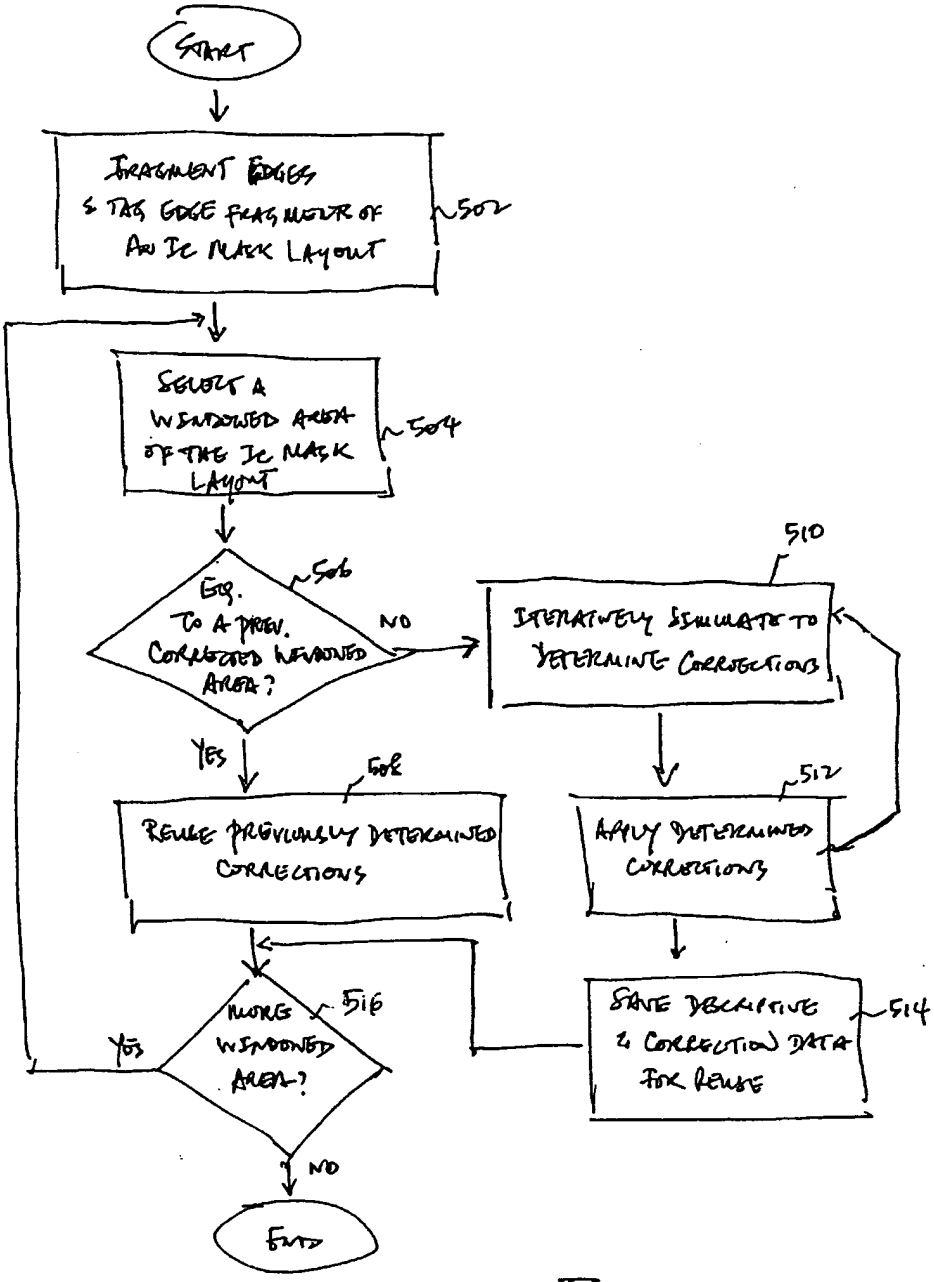

START
FRAGMENT EDGES & TAG EDGE FRAGMENTS OF AN IC MASK LAYOUT
502
SELECT A WINDOWED AREA OF THE IC MASK LAYOUT
504
EQ. TO A PREV. CORRECTED WINDOWED AREA?
506
NO
YES
ITERATIVELY SIMULATE TO DETERMINE CORRECTIONS
510
APPLY DETERMINED CORRECTIONS
512
STORE DESCRIPTIVE & CORRECTION DATA FOR REUSE
514
REUSE PREVIOUSLY DETERMINED CORRECTIONS
508
MORE WINDOWED AREA?
516
YES
NO
END

Fig. 5

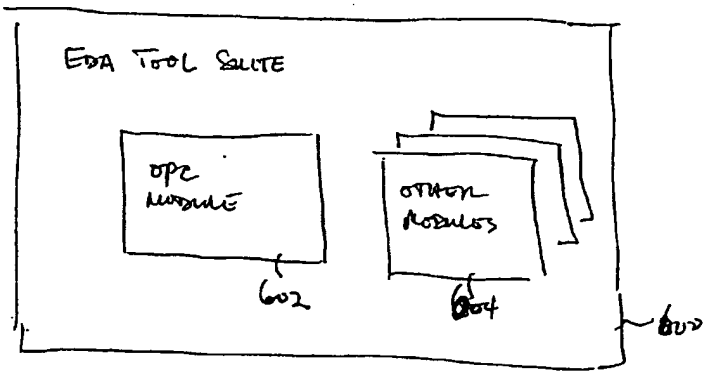

EDA TOOL SUITE
OPC MODULE
OTHER MODULES
602
604
600

FIG. 6

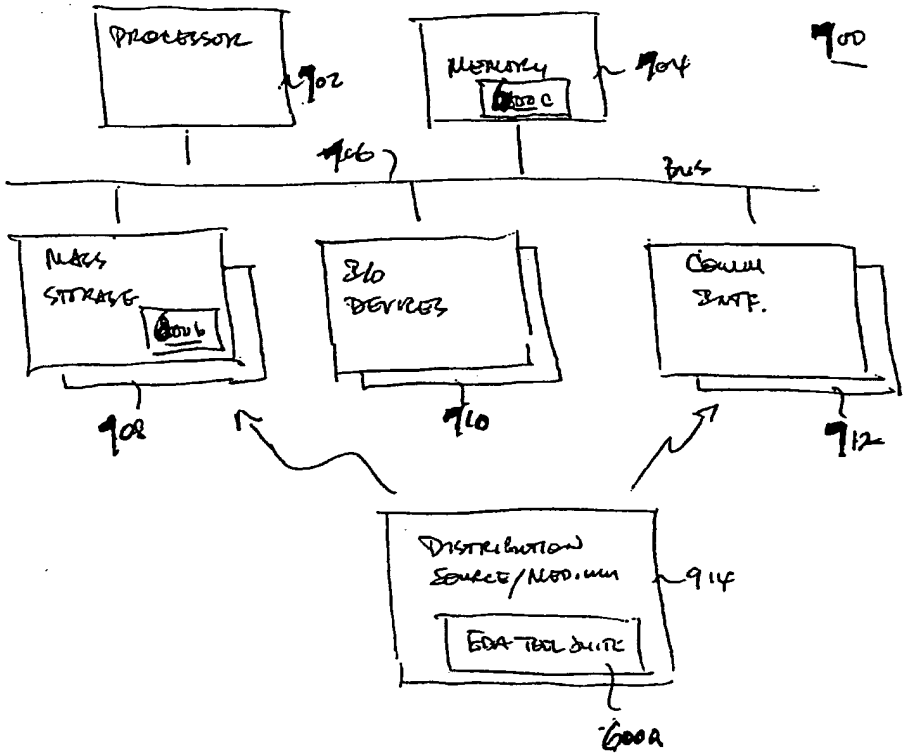

PROCESSOR
902
MEMORY
904
900
CODE C
906
BUS
MASS STORAGE
CODE B
908
I/O DEVICES
910
COMM INTF.
912
DISTRIBUTION SOURCE/MEDIUM
914
EDA TOOL SUITE
CODE A

FIG. 9

INTERNATIONAL SEARCH REPORT

Int: ional Application No
PCT/US 00/05658

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G03F7/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
INSPEC, WPI Data, PAJ, EPO-Internal, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MAURER W ET AL: "Process proximity correction using an automated software tool" , OPTICAL MICROLITHOGRAPHY XI, SANTA CLARA, CA, USA, 25-27 FEB. 1998 , PROCEEDINGS OF THE SPIE - THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING, 1998, SPIE-INT. SOC. OPT. ENG, USA, PAGE(S) 245 - 253 XP000933630 ISSN: 0277-786X	1-4,6, 8-15,17, 19-26, 28,30-33
Y	the whole document	7,18,29
	-/--	

[X] Further documents are listed in the continuation of box C. [ ] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 August 2000	31/08/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Haenisch, U

2

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/US 00/05658

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	MAURER W ET AL: "Evaluation of a fast and flexible OPC package: OPTISSIMO" , 16TH ANNUAL SYMPOSIUM ON PHOTOMASK TECHNOLOGY AND MANAGEMENT, REDWOOD CITY, CA, USA, 18-20 SEPT. 1996 , PROCEEDINGS OF THE SPIE - THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING, 1996, SPIE-INT. SOC. OPT. ENG, USA, PAGE(S) 412 - 418 XP000933628 ISSN: 0277-786X the whole document	1-4,6, 8-15,17, 19-26, 28,30-33
Y	OHNUMA H ET AL: "Lithography computer aided design technology for embedded memory in logic" MICROPROCESSES AND NANOTECHNOLOGY '98. 1998 INTERNATIONAL MICROPROCESSES AND NANOTECHNOLOGY CONFERENCE, KYOUNGJU, SOUTH KOREA, 13-16 JULY 1998, vol. 37, no. 12B, pages 6686-6688, XP000880238 Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers), Dec. 1998, Publication Office, Japanese Journal Appl. Phys, Japan ISSN: 0021-4922 page 6687, column 1, line 1 - line 25	7,18,29

2

Form PCT/ISA/210 (continuation of second sheet) (July 1992)